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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/808,031	03/23/2004	Takeshi Shimizu	073338.0114 (02-52471 FLA	5652

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EXAMINER	
RIYAMI, ABDULLA A	

ART UNIT	PAPER NUMBER
2609	

NOTIFICATION DATE	DELIVERY MODE
08/09/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/808,031	SHIMIZU, TAKESHI	
	Examiner	Art Unit	
	Abdullah Riyami	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,9-13,18 and 19* is/are rejected.

7)☒ Claim(s) *7,8,14-17 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1-6, 9-13, and 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakagawa (US 7245617 B2) in view of Christensen et al. (5491687).

In claim 1, Nakagawa teaches of a method in a high-speed switching environment (see column 2, lines 64-66), comprising: receiving, at a switch input port (see figure 2, block 24), a plurality of packets (see column 2, lines 64-66), including a first packet (see column 3, line 4) having at least first and second portions (see column 3, lines 3-12); initiating switching of the first portion before the entire second portion is received at the switch port (see column 3, lines 3-12); and of tag data associated with the first packet (see column 4, lines 51-65).

Nakagawa does not expressly disclose performing an error detection technique on the first packet using tag data associated with the first packet.

Christensen et al. discloses performing an error detection technique (see figure 2A, blocks 204, 208, 214, and 218 and column 5, lines 26-67 and column 6, lines 1-13) on the first packet using tag data associated with the first packet (see column 5, lines 26-67 and column 6, lines 1-13).

Nakagawa and Christensen et al. are analogous art because they are from the same field of endeavor of cut-through switching.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use Christensen et al.'s error detection technique (see figure 2A, blocks 204, 208, 214, and 218 and column 5, lines 26-67 and column 6, lines 1-13) in Nakagawa's high-speed switching environment (see column 2, lines 64-66).

The motivation to combine would have been to have a cut-forwarding switch capable of providing reduced latency, reduced memory requirements, and increased throughput, wherein frames/packets are examined for errors as the frames are passed through the ports. Hence, measures related to saving bandwidth can be taken when transferring frames/packets containing errors.

In claim 2, Nakagawa teaches of a method in a high-speed switching environment (see column 2, lines 64-66), wherein the initiating switching of the first portion is accomplished in accordance with a cut-through forwarding technique (see column 3, lines 3-12).

In claim 3, Nakagawa teaches of a method in a high-speed switching environment (see column 2, lines 64-66), wherein the initiating switching of the first portion is accomplished in accordance with a delayed cut-through forwarding technique (see column 8, lines 35-47).

In claim 4, Nakagawa teaches of a method in a high-speed switching environment (see column 2, lines 64-66) comprising looking up a tag ID (see column 4, lines 51-67) for association with the first packet (see column 4, lines 51-67).

In claim 5, Nakagawa teaches of a method in a high-speed switching environment (see column 2, lines 64-66), further comprising assigning the tag ID for association with the first packet (see column 4, lines 51-67).

In claim 6, Nakagawa teaches of a method in a high-speed switching environment (see column 2, lines 64-66), receiving the first portion (see column 3, lines 3-13) at a switch output port (see figure 2, block 24) but does not expressly disclose the error detection (see column 5) is performed at the switch output port.

Christensen et al. teaches of a method further comprising, receiving the first portion at a switch output port, wherein the error detection (see column 5) is performed at the switch output port (see figure 1, port 76 or 78 or 74, can all be output ports).

Nakagawa and Christensen et al. are analogous art because they are from the same field of endeavor of cut-through switching.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use Christensen et al.'s error detection technique (see figure 2A, blocks 204, 208, 214, and 218 and column 5, lines 26-67 and column 6, lines 1-13) in Nakagawa's high-speed switching environment (see column 2, lines 64-66) at the output port of the switch (see figure 2, block 24).

The motivation to combine would have been to have a cut-forwarding switch capable of providing reduced latency, reduced memory requirements, and increased throughput, wherein frames/packets are examined for errors as the frames are passed through the ports. Hence, measures related to saving bandwidth can be taken when transferring frames/packets containing errors.

In claim 9, Nakagawa teaches of a system in a high-speed switching environment (see column 2, lines 64-66), comprising: a first switch input port (see figure 2, block 24), being operable to receive a plurality of packets (see column 2, lines 64-66), including a first packet (see column 3, line 4) having first and second portions (see column 3, lines 3-12); a switch core (see figure 3) operable to switch the first portion before the entire second portion is received at the switch port (see column 3, lines 3-12); and of tag data associated with the first packet (see column 4, lines 51-65).

Nakagawa does not expressly disclose a detection module operable for performing an error detection technique on the first packet using tag data associated with the first packet.

Christensen et al. discloses a detection module (see figure 2A, blocks 204, 208, 214, and 218 and column 5, lines 26-67 and column 6, lines 1-13) operable for performing an error detection technique (see figure 2A, blocks 204, 208, 214, and 218 and column 5, lines 26-67 and column 6, lines 1-13) on the first packet using tag data associated with the first packet (see column 5, lines 26-67 and column 6, lines 1-13).

Nakagawa and Christensen et al. are analogous art because they are from the same field of endeavor of cut-through switching.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use Christensen et al.'s detection module (see figure 2A, blocks 204, 208, 214, and 218 and column 5, lines 26-67 and column 6, lines 1-13) operable for performing an error detection technique (see figure 2A, blocks 204, 208, 214, and 218 and column 5, lines 26-67 and column 6, lines 1-13) in Nakagawa's high-speed switching environment (see column 2, lines 64-66). The motivation to combine would have been to have a cut-forwarding switch capable of providing reduced latency, reduced memory requirements, and increased throughput, wherein frames/packets are examined for errors as the frames are passed through the ports. Hence, measures related to saving bandwidth can be taken when transferring frames/packets containing errors.

In claim 10, Nakagawa teaches of a system in a high-speed switching environment (see column 2, lines 64-66) comprising looking up a tag ID (see

column 4, lines 51-67) for association with the first packet (see column 4, lines 51-67).

In claim 11, Nakagawa teaches of a system in a high-speed switching environment (see column 2, lines 64-66), further comprising assigning the tag ID for association with the first packet (see column 4, lines 51-67).

In claim 12, Nakagawa teaches of a system in a high-speed switching environment (see column 2, lines 64-66) comprising, receiving the first portion (see column 3, lines 3-13) of the first packet at a switch output port (see figure 2, block 24).

In claim 13, Nakagawa teaches of a system in a high-speed switching environment (see column 2, lines 64-66), receiving the first portion (see column 3, lines 3-13) at a switch output port (see figure 2, block 24) but does not expressly disclose the switch output port comprising the error detection module (see column 5).

Christensen et al. teaches of a system, wherein the switch output port (see figure 1, port 76 or 78 or 74, can all be output ports) comprises the error detection module (column 5).

Nakagawa and Christensen et al. are analogous art because they are from the same field of endeavor of cut-through switching.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use Christensen et al.'s error detection module (see figure 2A, blocks 204, 208, 214, and 218 and column 5, lines 26-67 and column 6, lines 1-

13) in Nakagawa's high-speed switching environment (see column 2, lines 64-66) at the output port of the switch (see figure 2, block 24).

The motivation to combine would have been to have a cut-forwarding switch capable of providing reduced latency, reduced memory requirements, and increased throughput, wherein frames/packets are examined for errors as the frames are passed through the ports. Hence, measures related to saving bandwidth can be taken when transferring frames/packets containing errors.

In claim 18, Nakagawa teaches of a system in a high-speed switching environment (see column 2, lines 64-66), comprising: one or more memory structures (see figure 4 and column 12, lines 1-22); a plurality of input structures (see figure 4, block 38 and figure 3, port module) that are each operable to receive a packet (see column 3, lines 21-67) communicated from a component of a communications network and write the received packet (see column 3, lines 21-67) to one or more of the one or more memory structures (see figure 4 and figure 3, stream memory and columns 12-14); a first switching structure (see figure 3, blocks 28 on the left side) coupling the plurality of input structures to the one or more memory structures (see figure 4 and column 12, lines 1-22) such that each of the plurality of input structures are operable to write to each of the one or more memory structures (see column 5 and figures 3 and 4);

a plurality of output structures (see figure 3, port modules on the right side, and figure 4, blocks 38) that are each operable to read a packet (see column 3, lines 21-67) from one or more of the one or more memory structures (see figure 4 and

figure 3, stream memory and columns 12-14) for communication to a component of the communications network; a second switching structure (see figure 3, port modules on the right side, and figure 4, blocks 38) coupling the plurality of output structures to the one or more memory structures (see figure 4 and figure 3, stream memory and columns 12-14) such that each of the plurality of output structures are operable to read (see column 3, lines 21-67) from each of the one or more memory structures (see column 12-14), an output structure being operable to read a first portion of one of the packets from one or more of the one or more memory units (see column 4) for communication to a first component of the communications network before an input structure has received a second portion of the one of the packets communicated from a second component of the communications network (see column 3, lines 52-67); and of tag data associated with the first packet (see column 4, lines 51-65).

Nakagawa does not expressly disclose a detection module operable for performing an error detection technique on the first packet using tag data associated with the first packet.

Christensen et al. discloses a detection module (see figure 2A, blocks 204, 208, 214, and 218 and column 5, lines 26-67 and column 6, lines 1-13) operable for performing an error detection technique (see figure 2A, blocks 204, 208, 214, and 218 and column 5, lines 26-67 and column 6, lines 1-13) on the first packet using tag data associated with the first packet (see column 5, lines 26-67 and column 6, lines 1-13).

Nakagawa and Christensen et al. are analogous art because they are from the same field of endeavor of cut-through switching.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use Christensen et al.'s detection module (see figure 2A, blocks 204, 208, 214, and 218 and column 5, lines 26-67 and column 6, lines 1-13) operable for performing an error detection technique (see figure 2A, blocks 204, 208, 214, and 218 and column 5, lines 26-67 and column 6, lines 1-13) in Nakagawa's high-speed switching environment (see column 2, lines 64-66). The motivation to combine would have been to have a cut-forwarding switch capable of providing reduced latency, reduced memory requirements, and increased throughput, wherein frames/packets are examined for errors as the frames are passed through the ports. Hence, measures related to saving bandwidth can be taken when transferring frames/packets containing errors.

In claim 19, Nakagawa teaches of a system in a high-speed switching environment (see column 2, lines 64-66), wherein the memory structures are operable to store tag IDs for association with the packets (see column 4, lines 51-65).

Allowable Subject Matter

4. Claim 7-8, 14-17 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

	Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
A	US-7,042,891 B2	05-2006	Oberman et al.	370/412
B	US-6,049,546 A	04-2000	Ramakrishnan, Kadangode K.	370/412
C	US-6,091,707 A	07-2000	Egbert et al.	370/229
D	US-2001/0017866 A1	08-2001	Takada et al.	370/535
E	US-6,353,596 B1	03-2002	Grossglauser et al.	370/256
F	US-6,356,548 B1	03-2002	Nellenbach et al.	370/362
G	US-2002/0118692 A1	08-2002	Oberman et al.	370/419
H	US-6,687,247 B1	02-2004	Wilford et al.	370/392
I	US-6,781,994 B1	08-2004	Nogami et al.	370/395.1
J	US-2004/0179527 A1	09-2004	Cypher, Robert E.	370/392
K	US-6,922,749 B1	07-2005	Gil et al.	710/316
L	US-2005/0163051 A1	07-2005	Saito, Masahiro	370/235
M	US-2004/0156376	08-204	Nakagawa, Yukihiro	370/412

All of the references mentioned above are cited to show a cut-through forwarding technique for high speed switching.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abdullah Riyami whose telephone number is (571) 270-3119. The examiner can normally be reached on Monday through Thursday 8am-5pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dang Ton can be reached on (571) 272-3171. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AR

DANG T. TON
SUPERVISORY PATENT EXAMINER